Thermal Optimization of a Flip-Chip WiFi RF Front-End IC

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***Abstract* — Flip-chip designs offer several advantages over traditional designs. However, thermal characteristics must be considered carefully, or the end result may have high junction temperatures and thus poor performance and poor reliability. This paper presents some guidelines for thermal optimization in flip-chip designs, and presents the results of a flip-chip single die WiFi FEM developed using Bi-FET (HBT+E/D-PHEMT) technology. In this design, both solder bumps and copper pillar bumps were developed for the flip chip process.**

***Index Terms* — Copper Pillar, Flip-Chip, Front-End IC, Solder Bump, Thermal Optimization, WiFi.**

I. Introduction

To save cost, designers minimize die size and integrate as many features as possible on a die [1]. One way to reduce system size is to utilize flip-chip technology. Flip chip designs have a number of advantages over traditional chip-and-wire designs. These advantages include reduced overall cost, reduced module size, and simplified assembly. One disadvantage is that a flip-chip die is larger than a chip-and-wire die (due to increased pad sizes and pad pitch requirements). However the die size increase is usually a good compromise since the overall module using the chip can be smaller. Another flip-chip disadvantage is that the thermal characteristics of the die are typically worse than those of a standard chip-and-wire die.

Even though the flip-chip format has inherently worse thermal characteristics, the thermal performance can be improved using thermal analysis and careful layout. This paper will compare the thermal properties of flip-chip designs to traditional designs and discuss some of the ways to optimize thermal characteristics. Then the performance of a flip-chip WiFi front-end will be shown.

II. Flip Chip Details

Both solder bump and copper pillar versions of the flip-chip process were developed for this design. Solder bump is the more conventional form of flip chip processing and is probably the most widely used flip-chip process today. One advantage of the copper pillar flip-chip process it that it can utilize a smaller bump pitch than normal solder bumps.

A. Solder Bumps

For the solder bump process, the bump pitch was 200um and the bump diameter was ~120um. Nominal solder bump height was 85um. Fig. 1 shows a diagram of the solder bump used for this design. Tin was used as the solder material in this design. Fig. 2 shows a photograph of some typical solder bumps.

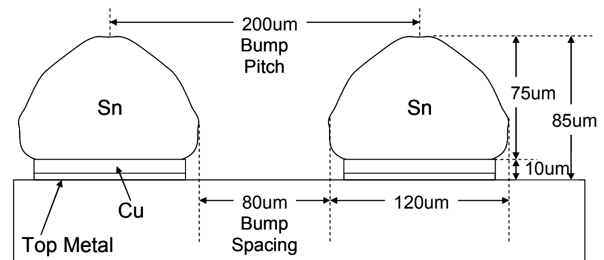

Fig. 1. Profile of solder bumps used in this flip-chip design.

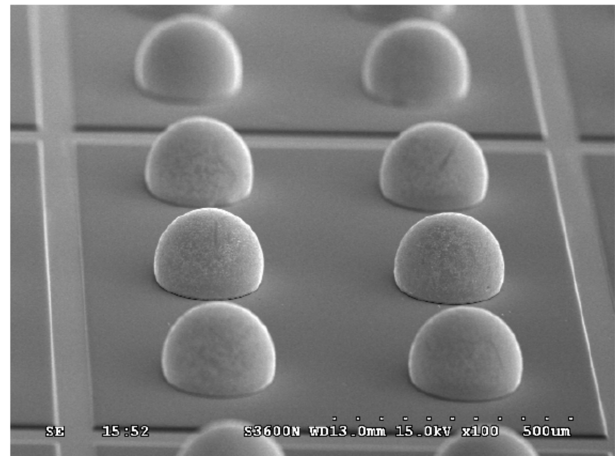

Fig. 2. Photo of Sn-Ag Solder Bumps.

B. Copper Pillar

For the copper pillar bump process, the bump pitch was also 200um and the bump diameter was ~105um. The total bump height was 85um including a ~50um high pillar and a ~35um high (Sn) solder cap. Fig. 3 shows a profile of the copper pillar used for this design, and Fig. 4 shows a photograph of a typical copper pillar.

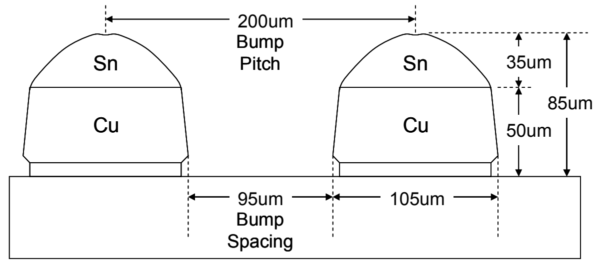

Fig. 3. Profile of copper pillar bumps used in this design.

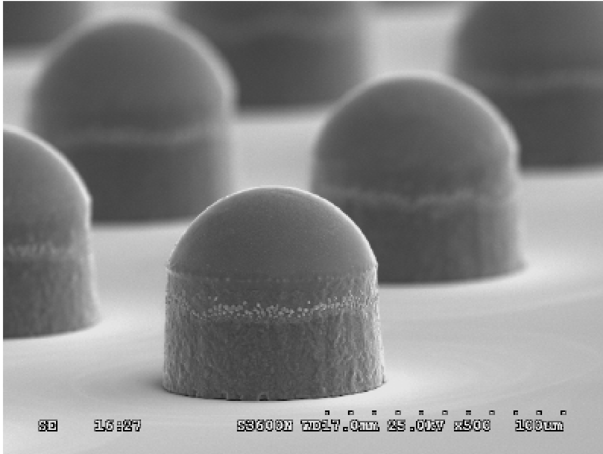

Fig. 4. Photo of copper pillar bumps.

III. Thermal Analysis & Optimization

To improve the performance and reliability and to help develop flip-chip layout rules, thermal analyses of the front-end IC were performed for different manufacturing formats (traditional chip-and-wire, flip-chip, and flip-chip with underfill). For each simulated case considered, the die dissipates a total power of 500 mW (which generally corresponds to RF output power of 20 dBm at 20% efficiency). The baseplate temperature is set to 70°C. Note that the simulations are based on the existing die design. Using what was learned during the simulations and tests, the layout could be modified and additional improvement to thermal characteristics could be achieved.

The baseline case is the traditional chip-and-wire format. In this case, most of the heat flows vertically down through the GaAs substrate toward the baseplate (thermal ground). The heat does not spread very much horizontally. The best ways to minimize the junction temperature are to use a thin die and to space the transistor fingers as far apart as possible. Fig. 5 illustrates a case where all of the transistor fingers are close together, resulting is a high junction temperature at the center of the transistor. Fig. 6 illustrates the case where the transistor fingers are spread, resulting in a lower junction

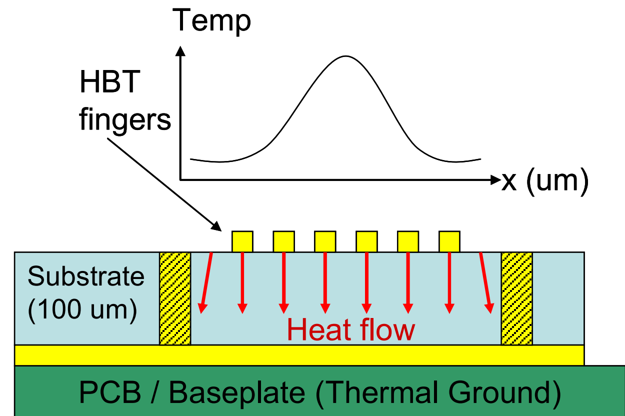

Fig. 5. Illustration of heat flow and junction temperature of a normal die (wirebond form). Most heat flows vertically through the GaAs substrate from the HBT fingers to the thermal ground. Junction temperature peaks at the center of the transistor.

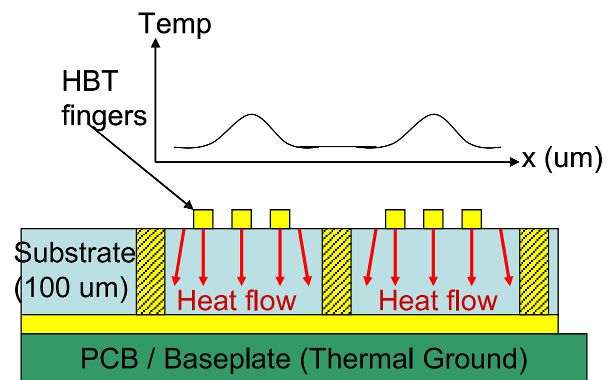

Fig. 6. Illustration of heat flow and junction temperature of a modified layout. Separating the transistor fingers reduces the maximum junction temperature.

temperature. The results of a thermal simulation for a chip-and-wire die indicate that the maximum junction temperature is 111.5°C, which corresponds to a thermal resistance θjc = 82°C/W.

For a flip-chip die, the heat spreads horizontally through the die until it reaches a good path to thermal ground (i.e. a bump or pillar) as shown in Fig. 7. For this case, the best ways to minimize junction temperature are to add more ground bumps and to space the transistor fingers as far apart as possible. Fig. 8 shows the results of a thermal simulation for a flip-chip die. These results indicate the maximum junction temperature is 121.6°C (baseplate=70°C), which corresponds to a thermal resistance θjc=102°C/W. Note that the maximum junction temperature for the flip chip die is approximately 10°C hotter than the chip-and-wire die for the same power dissipation. This shows the importance of taking thermal

performance into account during the flip-chip design process.

Underfill material is sometimes used to provide mechanical support and improve long term reliability of flip-chip die. It may also have some effect on junction temperature by providing an additional path to thermal ground. Unfortunately, most underfill materials have poor thermal characteristics, and it is still very important to use good layout techniques such as spacing transistor fingers far apart and using lots of ground bumps. This case is illustrated in Fig. 9, and Fig. 10 shows the thermal simulation results of a flip-chip die with underfill. The results indicate a max junction temperature of 118°C which corresponds to a thermal resistance θjc = 96°C/W.

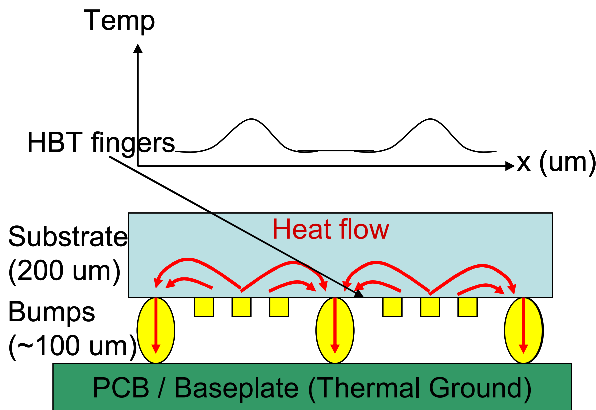

Fig. 7. Illustration of heat flow and junction temperature of a flip-chip die. Most heat flows horizontally until a good path to thermal ground (i.e. bump) is encountered.

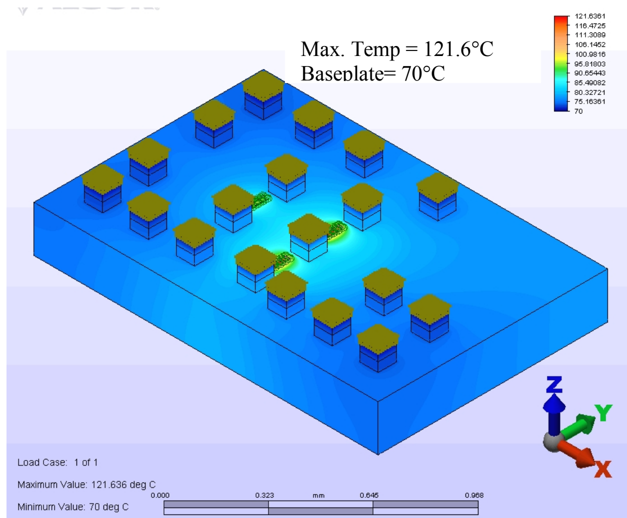

Fig. 8. Thermal model of a flip-chip front-end IC (no underfill). Model uses GaAs die with copper pillar bumps, 70°C baseplate temp, and 500 mW power dissipation. Maximum temperature is 121.6°C and thermal resistance is 102°C/W.

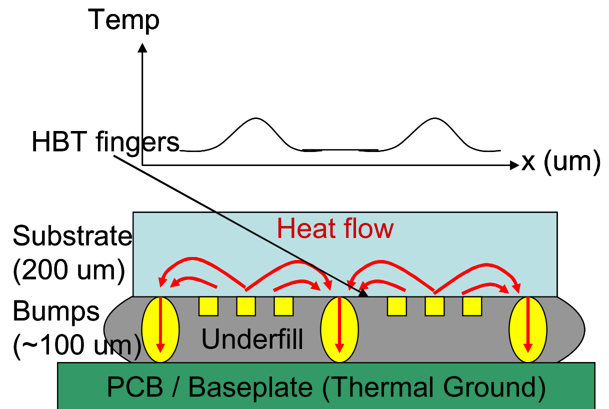

Fig. 9. Illustration of heat flow and junction temperature of a flip-chip die with underfill.

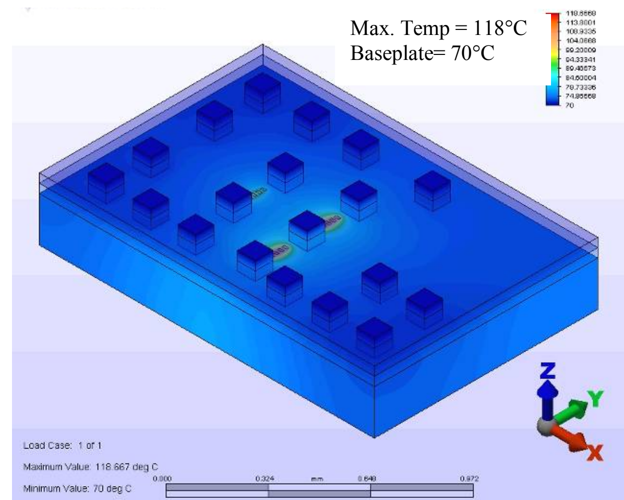

Fig. 10. Thermal model of a flip-chip front-end IC with underfill. Model uses GaAs die with copper pillar bumps, 70°C baseplate temp, and 500 mW power dissipation. Maximum temperature is 118°C and thermal resistance is 96°C/W.

II. RF PERFORMANCE

A flip-chip single-die WiFi FEM was developed using Bi-FET (HBT+E/D-PHEMT) technology. Both solder bumps and copper pillar bumps were developed for the flip chip process [2]. This FEM die consists of a high-pass filter (HPF), a 2GHz WiFi PA with on-chip regulator, PAON logic and detector circuit, and an SP3T. The HPF provides rejection for WCDMA at 2.17GHz. The 3-stage PA provides 33 dB gain with good linearity (3% EVM, 17dBm) and good efficiency (Icc=135mA @18dBm) for the FEM at the antenna port. The SP3T can be switched to connect the antenna port to the Tx port (PA output), Rx port, or BT port. A detector output is provided to monitor FEM output power. The FEM is biased by a single battery

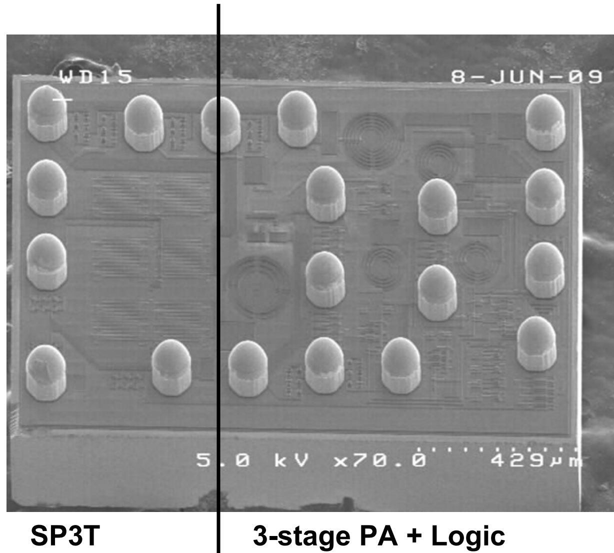

Fig. 11. Photo of FEIC die using copper pillars. The die size is 1.5 x 0.9 mm, and includes a HPF, PA, and SP3T.

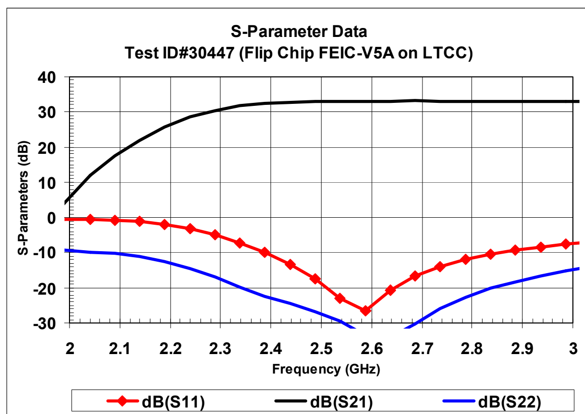

Fig. 12. Measured S-parameters for the flip-chip FEIC die.

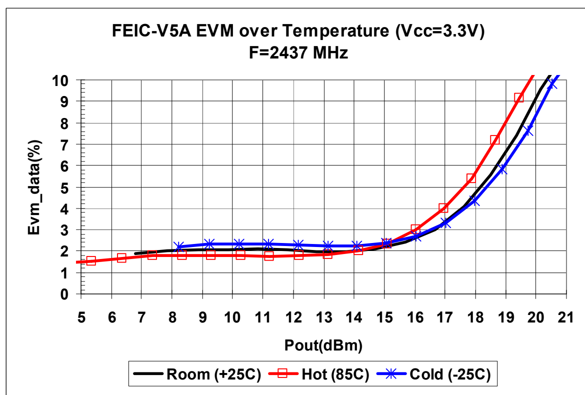

Fig. 13. Transmit mode EVM over Temp at 2.437 GHz.

supply (Vbat) from 2.3V to 4.8V. The digital command for PAON and SP3T control varies from 1.6V to 2.1V.A photograph of this flip chip FEM die using Cu-pillar bumps is shown in Fig. 11.

The S-parameter data of Tx mode at nominal bias (Vbat=3.3V, PAON=SP3T Vc2=1.8V) is shown in Fig. 12. The FEM has 33dB Gain and better than 15 dB return loss in band. The 2.17 GHz rejection can be improved by adjusting the external high Q notch inductor. For both the Rx and BT modes the insertion loss is around 0.7dB (at SP3T Vc1 or Vc3=1.8V) and return losses are better than 15dB in band.

From 2.412-2.484GHz, the EVM is less than 3% up to Pout=17dBm. The design has Icq=72mA and Icc=135mA @18dBm at Vcc=+3.3V. Excellent EVM and Icc over temperature data (at Cold -25°C, Room Temp and Hot +85°C) are shown in Fig. 13. The detector output variation over both bias supply range and over temperature is also very small. The flip-chip FEIC test data is as good as (or identical to) the FEIC die in wirebond form. This indicates that the flip-chip FEIC thermal design is good.

V. Conclusion

Flip chip designs offer many advantages over traditional chip and wire designs (cost, size, assembly). However, the thermal properties of flip-chip die must be considered early in the design process. Ignoring the thermal properties will result in high junction temperatures which will degrade both RF performance and long term reliability. By using the general layout guidelines presented here and good design practices (such as thermal simulation), the thermal characteristics of a flip-chip design can be optimized.

We have developed a flip chip WiFi FEM die with good RF and thermal performance. This flip-chip FEM die enables size and cost reduction in the final application.

References

[1] C. Yuen, "Low Cost, Highly Integrated FEMs for Low Current and High Output Power WLAN Applications," Presented at IMS2005 Workshop-WSD, *2005 IEEE MTT-S International Microwave Symposium Digest*, Long Beach, CA, June 12, 2005

[2] C.Yuen, K. Laursen, D. Chu, H. Do, H. Chen, Y.-C. Pao, "A Compact Flip Chip Single Die WiFi FEM for Smart Phone Application", in *IEEE Topical Symposium on Power Amplifiers for Wireless Communications*, San Diego, CA, Sept. 14, 2009